Kyle E. Powers

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EDUCATION

University of Virginia — ***Charlottesville, VA***
School of Engineering and Applied Science — **Aug. 2009 – May 2013**

- Bachelor of Science (B.S.) in Electrical Engineering, GPA – 3.18 (Major)
- Focus in Very Large Scale Integration (VLSI), variation tolerance, and high performance, low power research
- Relevant Courses – VLSI, Microfabrication, Solid State Devices, E&M Fields, Comp. Arch., Comp. Sci., Signals

ACADEMIC PROJECTS

Senior Technical Thesis, Lead Designer — **Aug. 2012 – Dec. 2012**

- Directed a team of three in *Improving the Superset Adder – A Fault-tolerant, Reconfigurable Prefix Adder*
- Created and maintained progress schedules; authored interim design reviews, final thesis, and presentation
- Produced gate-level diagrams in Logisim; recreated and verified designs at the transistor level in Cadence
- By exploiting "power gating" and the "inversion property" of adders, simulation results showed an increase in performance up to 10%, whilst reducing overall power consumption up to 8.9%, varying on configuration

Digital Signal Processor, Lead Designer — **Jan. 2012 – May 2012**

- Guided a team of five in designing a digital signal processor in FreePDK 45nm using Cadence Virtuoso; DSP required addition, subtraction, multiplication, shift, AND, OR on two 16-bit inputs with clocked registers
- Created and maintained progress schedules; authored interim design reviews, final paper, and presentation
- Increased addition performance by a factor of 12; reduced total DSP area 57.6% by combining ADD and SUB

Other Course Projects — **Aug. 2010 – Dec. 2011**

- Cooperated with a partner to design, simulate, build, and physically verify a DC coupled multi-stage amplifier
- Designed a gumball machine controller using a finite state machine with D flip-flops, encoder, and decoder
- Designer – Worked with a group of five to create a Java-based Google Chat I.M. Client using XMPP and Swing

UNDERGRADUATE RESEARCH

High-Performance Low-Power VLSI Lab — ***Charlottesville, VA***
NAND Flash Recovery, Independent Researcher — **Aug. 2012 – Dec. 2012**

- Utilizing the photoelectric effect of U.V. light, accelerated the charge detrapping process that occurs during the idle time between program/erase activities; results showed 25x/40x improvement for SLC/MLC, respectively

Design Methodologies, Co-researcher — **Jan. 2012 – May 2012**

- Investigated a new taxonomy for reconfigurable, fault-tolerant parallel prefix adders; explored the use of Arithmetic Description Language (ARITH), a language for translating arithmetic algorithms to HDL

WORK EXPERIENCE

Intel Corporation — ***Hudson, MA***
Yield Analysis – Defect Metrology, Intern — **May 2012 – Aug. 2012**

- Rapidly learned SQLPathFinder and Klarity to assemble defect data; utilized Excel/JMP for statistical analyses
- Developed 12 1Click! applications for Defect Metrology Layer Owners and for the Integrated Module teams; results were instrumental for F17 DEFMET's progression toward self-sustained manufacturing of P86x
- "I'm in. Intel Involved" – Volunteered with RCGnet and Community Harvest for local food donation

Manufacturing Technician, Intern — **May 2010 – Aug. 2010**

- Operated GaSonics tools that plasma etched the photoresist from silicon wafers in a Class 1 fabrication facility
- Created *Pocketable Reference*, an additional training aid and tool information reference for new employees
- Developed a system of categorization to increase production, yield rates, and active/passive communication

TECHNICAL SKILLS

- Software – Cadence, Logisim, LTSpice, MATLAB, Eclipse, FPGA Advantage, SQLPathFinder, JMP, Klarity
- Lab Hardware – Protoboards, multimeters, power supplies, oscilloscopes, function generators, SEM/AFMs
- Programming (Proficient || Knowledgeable) – Java, SQL, JSL || C++, VHSIC HDL, assembly, shell scripting